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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please amend claims 23 and 31-40 as follows:

Claims 1-22 (cancelled)

23. (currently amended): A system core comprising:

a processor;

a direct memory access (DMA) controller operating under control of a DMA processor;

an instruction memory containing processor instructions and DMA processor instructions;

a plurality of memories, the DMA controller coupled to the instruction memory and the plurality of memories, the DMA ~~controller~~ processor configured for fetching ~~and executing~~ the DMA instructions from the instruction memory and executing the DMA instructions in parallel with the processor fetching and executing the processor instructions, the DMA instructions when executed causing the transfer of data to populate the plurality of memories with data from an external device, the processor operating on the data found in the populated memories.

24. (previously presented): The system core of claim 23 wherein the executed DMA instructions specify a pattern to populate the plurality of memories.

25. (previously presented): The system core of claim 24 wherein the pattern is a block, circular, or stride pattern.

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26. (previously presented): The system core of claim 23 wherein the data from the external device includes processor instructions.

27. (previously presented): The system core of claim 23 further comprising:

a DMA bus connecting the DMA controller to the instruction memory and the plurality of memories.

28. (previously presented): The system core of claim 23 further comprising:

a bus coupled to the external device and the system core.

29. (previously presented): The system core of claim 23 wherein the external device is an external host processor.

30. (previously presented): The system core of claim 23 wherein the external device is an external synchronous data random access memory (SDRAM).

31. (currently amended): The system core of claim 23 wherein the DMA ~~controller~~ processor fetches ~~and executes~~ DMA instructions from the instruction memory and executes the DMA instructions in parallel with the processor fetching and executing the processor instructions, the DMA instructions when executed causing the transfer of data to populate the external device with data from the plurality of memories.

32. (currently amended): A method for transferring data between a system core and an external device, the system core having a processor, a direct memory access (DMA) processor, an instruction memory storing processor instructions and DMA processor instructions, and a plurality of memories, the method comprising:

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fetching direct memory access (DMA) instructions from the instruction memory under control of the DMA processor ;

executing the fetched DMA instructions in parallel with the processor fetching and executing the processor instructions, the DMA instructions when executed causing the transfer of data to populate the plurality of memories with data from the external device; and

transferring data from the external device to the plurality of memories.

33. (currently amended): The method of claim ~~31~~ 32 wherein the executed DMA instructions specify a pattern to populate the plurality of memories.

34. (currently amended): The method of claim ~~32~~ 33 wherein the pattern is a block, circular, or stride pattern.

35. (currently amended): The method of claim ~~31~~ 32 wherein the data from the external device includes processor instructions.

36. (currently amended): The method of claim ~~31~~ 32 wherein the external device is an external host processor.

37. (currently amended): The method of claim ~~31~~ 32 wherein the external device is an external synchronous data random access memory (SDRAM).

38. (currently amended): The method of claim ~~31~~ 32 further comprising:

executing the fetched DMA instructions in parallel with the processor fetching and executing the processor instructions, the DMA instructions when executed causing the transfer of data to populate the external device with data from the plurality of memories; and

transferring data from the plurality of memories to ~~from~~ the external device.

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39. (currently amended): The method of claim 38 wherein the transferring data step further comprises:

accessing data from the plurality of memories;

writing the data to the external device, wherein both ~~transferring~~ the accessing and the writing steps occur ~~simultaneously~~ in parallel.

40. (currently amended): The method of claim 32 wherein the ~~system core contains~~processor is a sequential processor (SP) which executes the data transferred from the external device as instructions.

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